

**ASSIGNMENT 7**

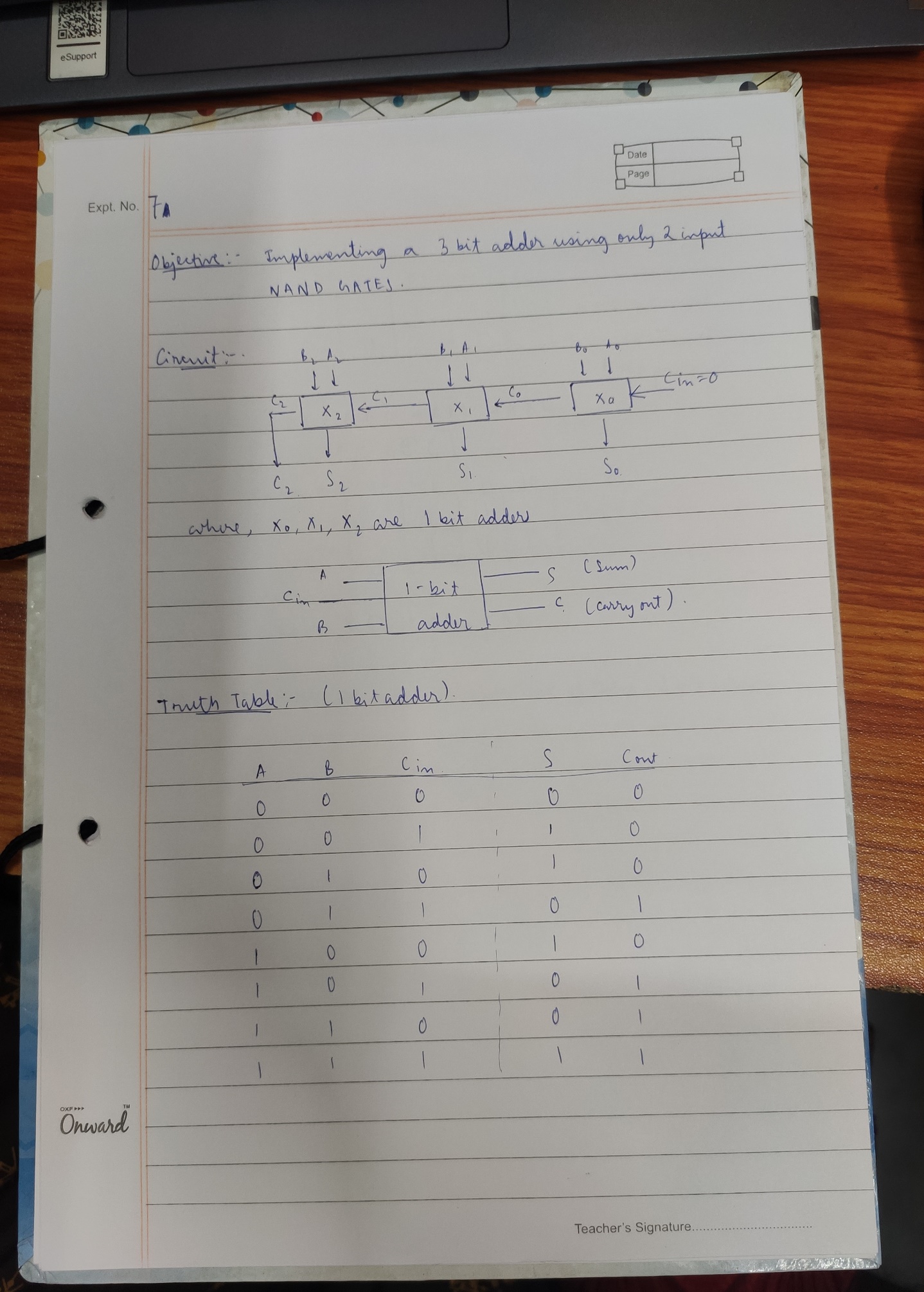
[Design of a combinational logic circuit for **3-BIT ADDER AND SUBTRACTOR** using 2 input NAND GATES]

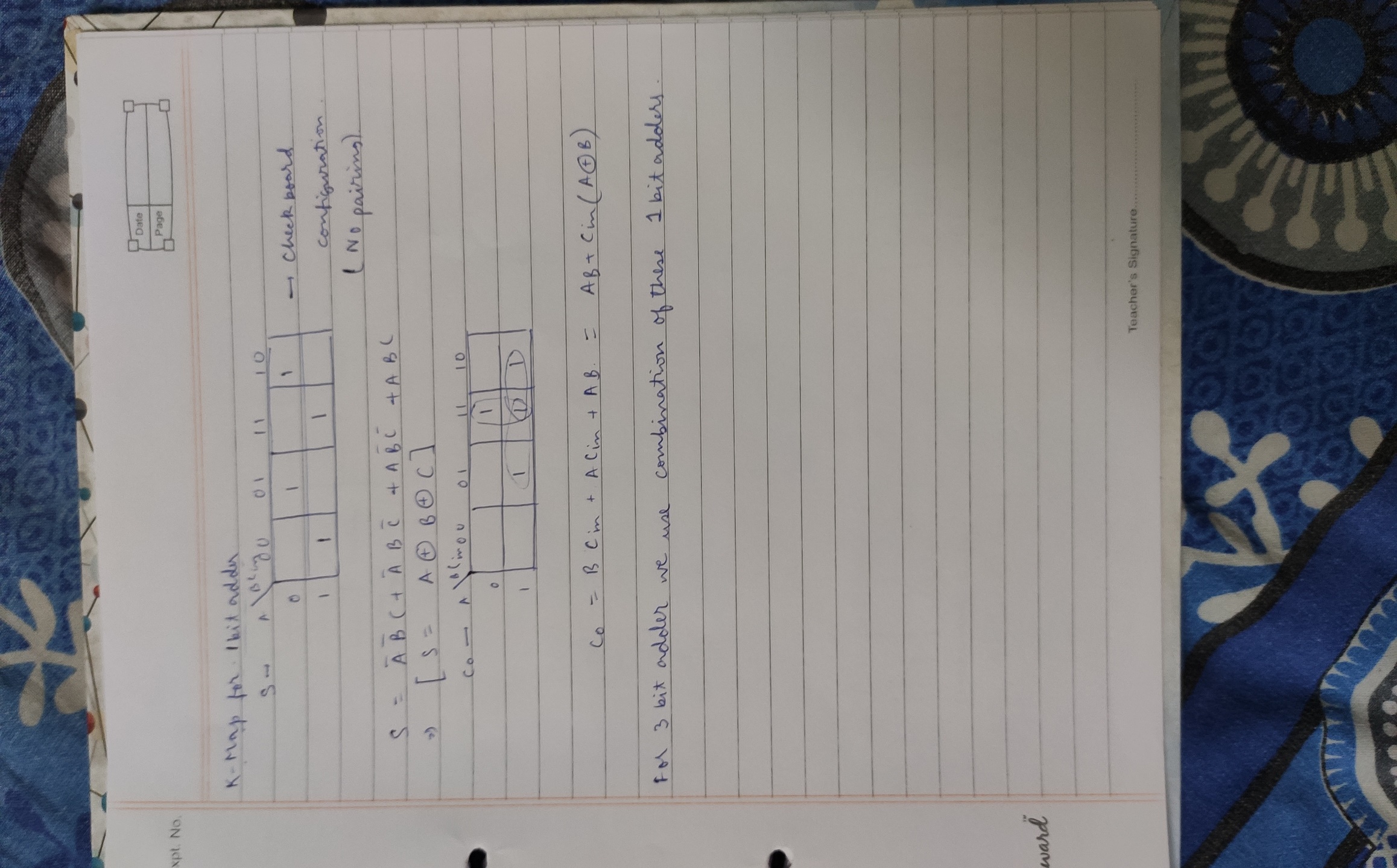


**NAME: ROHIT SADHU**

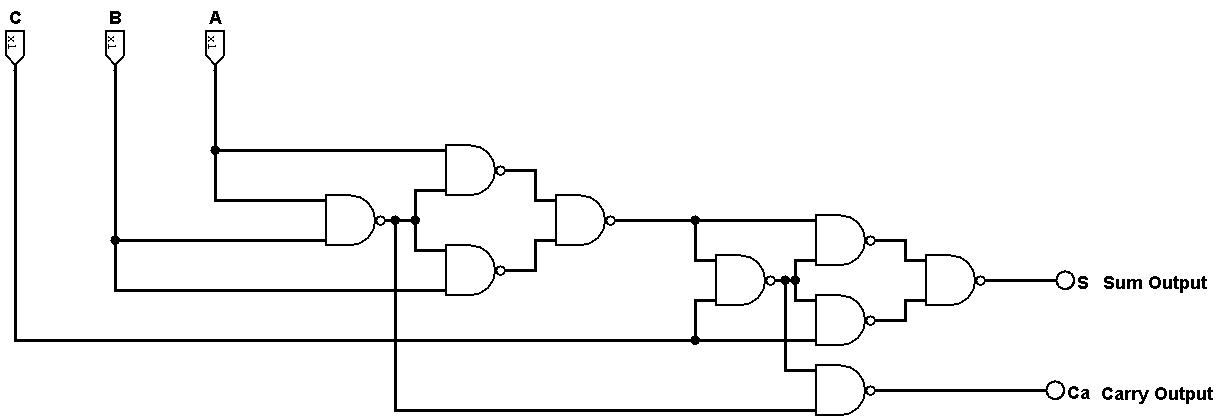
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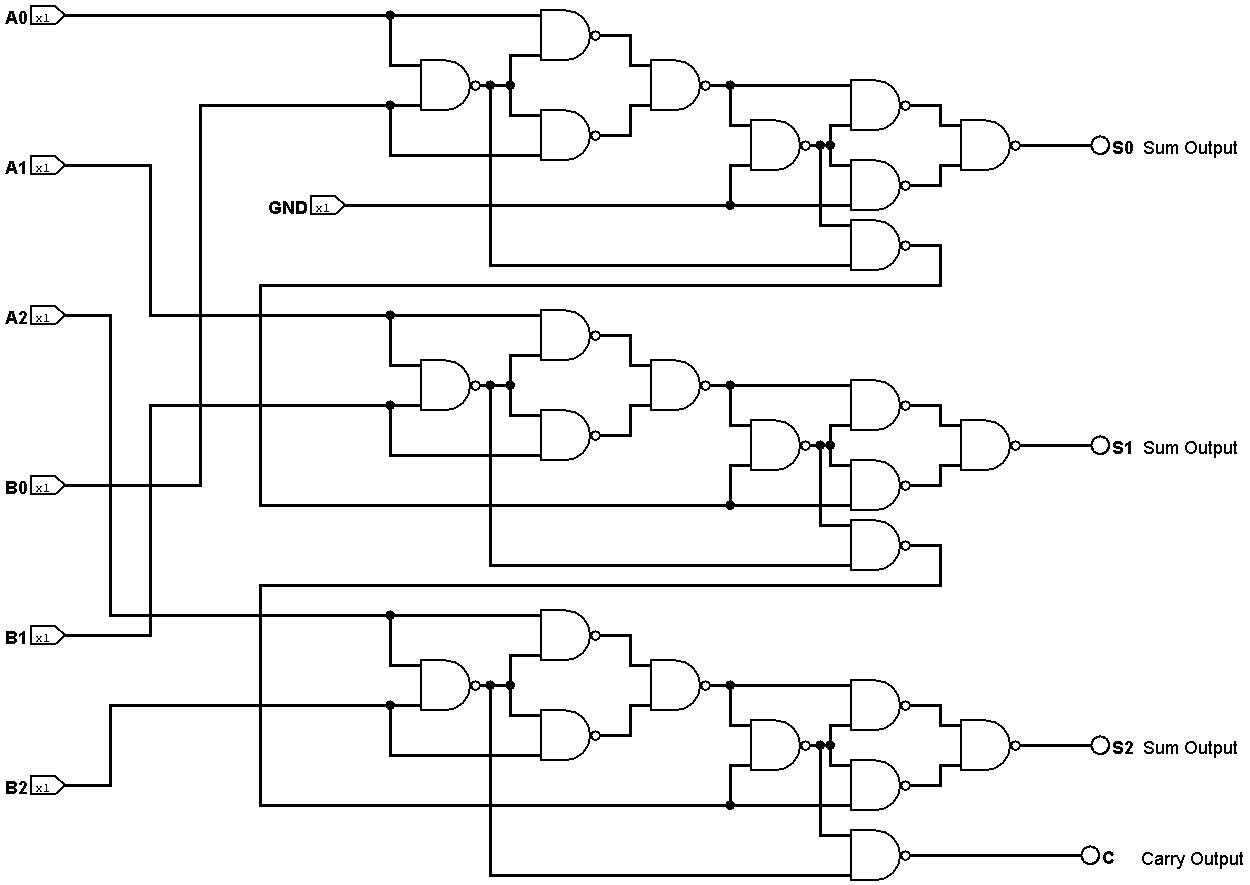


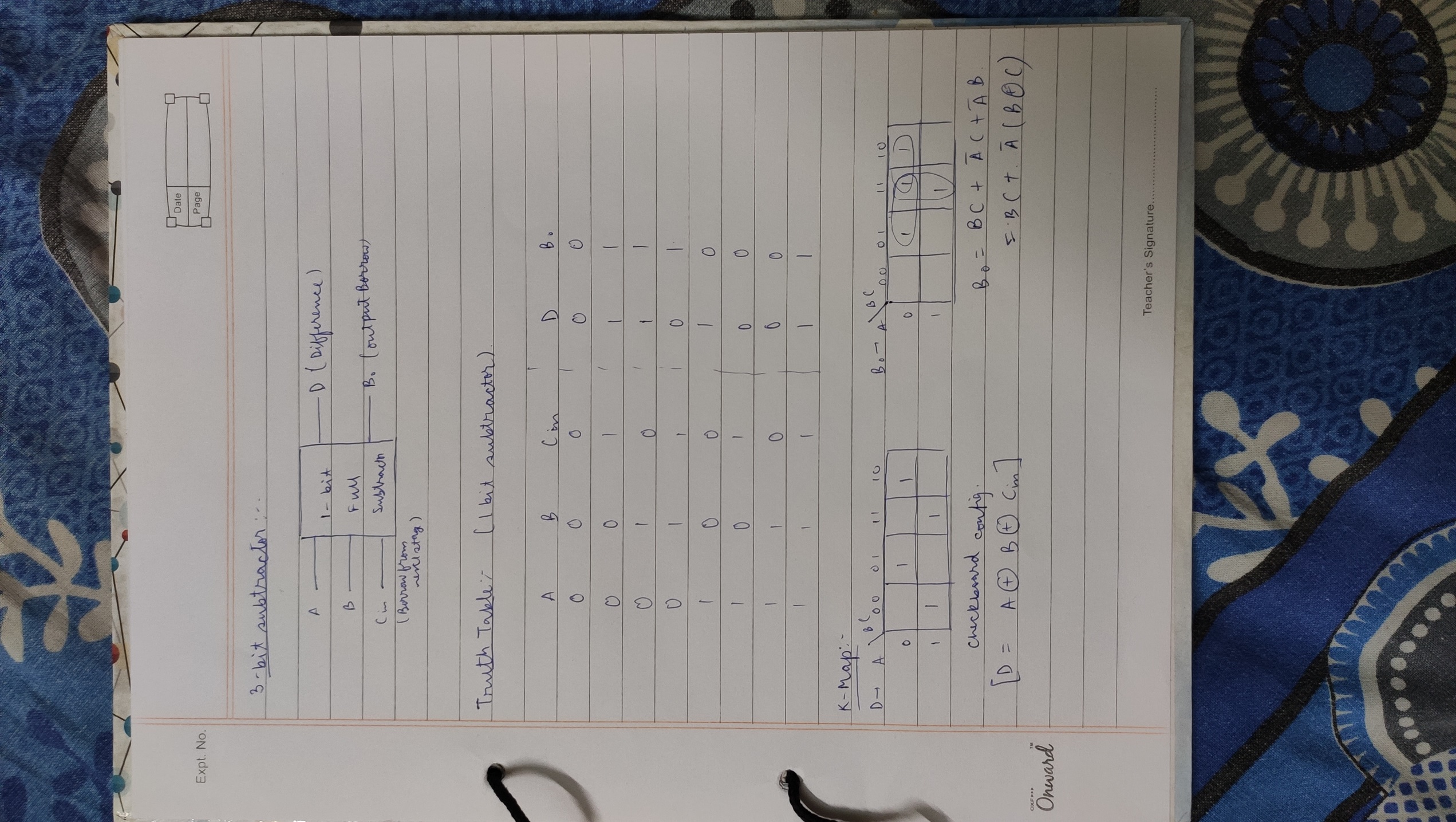




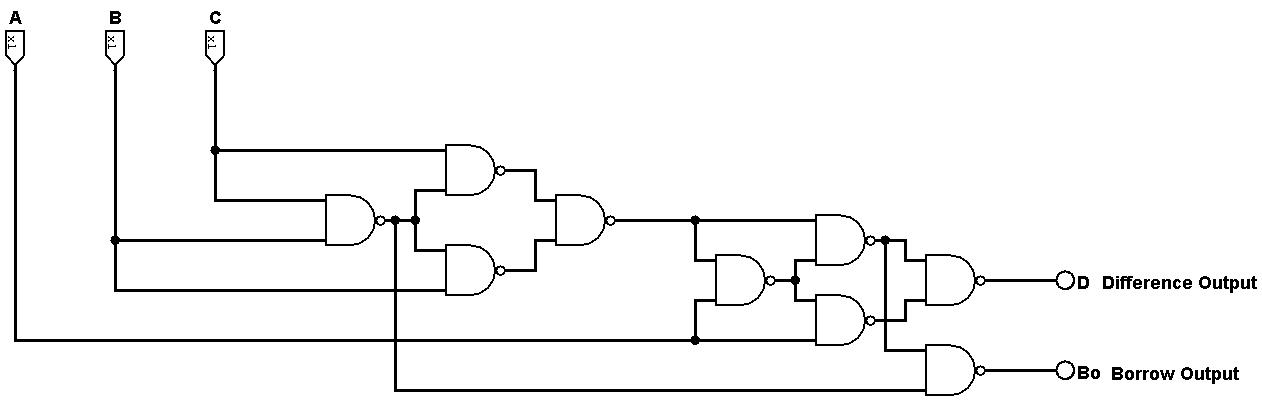
**CIRCUIT DIAGRAM:**

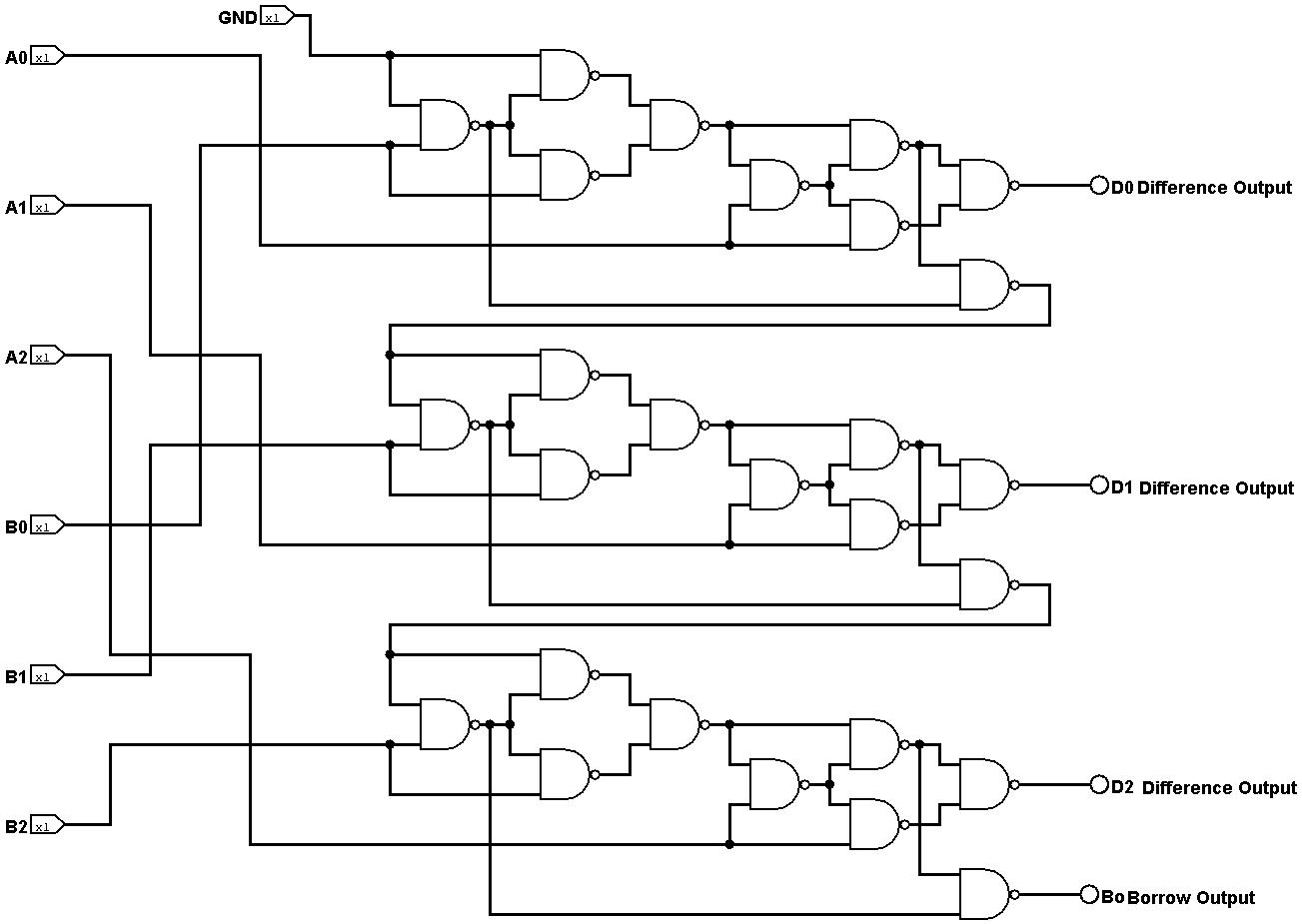
**1 BIT FULL ADDER:**

**3 BIT FULL ADDER:**



**CIRCUIT DIAGRAM:**

**1 BIT FULL SUBTRACTOR:**

**3 BIT FULL SUBTRACTOR:**